WHAT IS CLAIMED IS:

1. A semiconductor component comprising:

a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

a first die attached to the substrate, electrically connected to the interconnect contacts and encapsulated in a first encapsulant;

a second die attached to the first encapsulant and electrically connected to the interconnect contacts; and

a second encapsulant encapsulating the second die and the first encapsulant.

2. The semiconductor component of claim 1 wherein the first encapsulant comprises a molded plastic having a planar surface for the second die.

3. The semiconductor component of claim 1 further comprising a first adhesive layer adhesively bonding the first die to the substrate.

4. The semiconductor component of claim 1 further comprising a second adhesive layer adhesively bonding the second die to the first encapsulant.

5. The semiconductor component of claim 1 wherein the first encapsulant comprises at least one locking feature configured to increase adhesive bonding of the second die to the first encapsulant.

6. The semiconductor component of claim 1 further comprising a third die back bonded to the second encapsulant and wire bonded to the interconnect contacts.

7. The semiconductor component of claim 1 further comprising a plurality of first interconnects bonded to the first die and to the interconnect contacts, and a plurality of second interconnects bonded to the second die and to the interconnect contacts.

8. The semiconductor component of claim 7 wherein the first interconnects and the second interconnects comprise wire bonded wires.

9. The semiconductor component of claim 7 wherein the first interconnects and the second interconnects comprise TAB bonded tape.

10. A semiconductor component comprising:

a substrate comprising a plurality of first interconnect contacts and a plurality of second interconnect contacts;

a first die attached to the substrate comprising a plurality of first die contacts;

a plurality of first interconnects bonded to the first die contacts and to the first interconnect contacts;

a first encapsulant encapsulating the first die and the first interconnects but shaped to not encapsulate the second interconnect contacts;

a second die attached to the first encapsulant comprising a plurality of second die contacts;

a plurality of second interconnects bonded to the second die contacts and to the second interconnect contacts; and

a second encapsulant encapsulating the second die, the second interconnects and the first encapsulant.

11. The semiconductor component of claim 10 wherein the second interconnect contacts are located proximate to a

peripheral edge of the substrate and the second interconnect contacts are located proximate to an inner portion of the substrate.

12. The semiconductor component of claim 10 wherein the first interconnect contacts and the second interconnect contacts are arranged in spaced rows on opposing edges of the substrate.

13. The semiconductor component of claim 10 further comprising a first adhesive layer attaching the first die to the substrate.

14. The semiconductor component of claim 10 further comprising a second adhesive layer attaching the second die to the first encapsulant and at least one locking feature on the first encapsulant configured to promote adhesion of the second adhesive layer to the first encapsulant.

15. The semiconductor component of claim 10 wherein the first interconnects and the second interconnects comprise wire bonded wires.

16. The semiconductor component of claim 10 wherein the first interconnects and the second interconnects comprise bonded TAB tape.

17. The semiconductor component of claim 10 further comprising a plurality of terminal contacts on the substrate in electrical communication with the first interconnect contacts and the second interconnect contacts.

18. The semiconductor component of claim 10 further comprising a third die attached to the second encapsulant

and a third encapsulant encapsulating the third die and the second encapsulant.

19. A semiconductor component comprising:

a substrate comprising a plurality of terminal contacts on an outer surface thereof, and a plurality of interconnect contacts on an inner surface thereof in electrical communication with the terminal contacts;

a first die back bonded to the substrate;

a plurality of first interconnects bonded to the first die and to the interconnect contacts;

a first encapsulant encapsulating the first die and the first interconnects;

a second die back bonded to the first encapsulant;

a plurality of second interconnects bonded to the second die and to the interconnect contacts; and

a second encapsulant encapsulating the second die, the second interconnects, and the first encapsulant.

20. The semiconductor component of claim 19 wherein the interconnect contacts comprise first interconnect contacts for the first die and second interconnect contacts for the second die located outside of the first encapsulant.

21. The semiconductor component of claim 19 wherein the first encapsulant comprises a molded plastic having a planar surface.

22. The semiconductor component of claim 19 wherein the second encapsulant comprises a plurality of molded locking features configured to facilitate adhesive bonding of the second die.

23. The semiconductor component of claim 19 further comprising a first adhesive layer adhesively bonding the first die to the substrate.

24. The semiconductor component of claim 19 further comprising a second adhesive layer adhesively bonding the second die to the first encapsulant.

25. The semiconductor component of claim 19 wherein the first interconnects and the second interconnects comprise wire bonded wires.

26. The semiconductor component of claim 19 wherein the first interconnects and the second interconnects comprise tape.

27. The semiconductor component of claim 19 further comprising a third die back bonded to the second encapsulant and a third encapsulant encapsulating the third die and the second encapsulant.

28. A semiconductor component comprising:

a substrate comprising a plurality of terminal contacts on an outer surface thereof and a plurality of first interconnect contacts on an inner surface thereof in electrical communication with the terminal contacts;

a first die adhesively attached to the inner surface comprising a plurality of first die contacts;

a plurality of first interconnects bonded to the first interconnect contacts and to the first die contacts;

a first encapsulant shaped to encapsulate the first die and the first interconnects but not the second interconnect contacts;

a second die adhesively bonded to the first encapsulant comprising a plurality of second die contacts;

a plurality of second interconnects bonded to the second interconnect contacts and to the second die contacts; and

a second encapsulant encapsulating the second die, the second interconnects and the first encapsulant.

29. The semiconductor component of claim 28 wherein the first encapsulant has a first peripheral outline larger than the die but within a perimeter formed by the second interconnect contacts.

30. The semiconductor component of claim 28 wherein the second encapsulant has a second peripheral outline matching that of the substrate.

31. The semiconductor component of claim 28 wherein the first encapsulant comprises at least one locking feature comprising a molded ridge, a dimple, an indentation, or a groove.

32. The semiconductor component of claim 28 further comprising a first adhesive layer adhesively bonding the first die to the substrate.

33. The semiconductor component of claim 28 further comprising a second adhesive layer adhesively bonding the second die to the substrate.

34. The semiconductor component of claim 28 wherein the first interconnects and the second interconnects comprise wire bonded wires.

35. The semiconductor component of claim 28 wherein the first interconnects and the second interconnects comprise TAB bonded tape.

36. The semiconductor component of claim 28 wherein the terminal contacts comprise bumps or balls in an area array.

37. A semiconductor component comprising:

a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

at least one die stack on the substrate comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die, and a second die bonded to the first encapsulant in electrical communication with the interconnect contacts; and

a second encapsulant on the substrate encapsulating the die stack.

38. The semiconductor component of claim 37 wherein the first die and the second die are wire bonded to the interconnect contacts.

39. The semiconductor component of claim 37 wherein the first die and the second die are TAB bonded to the interconnect contacts.

40. The semiconductor component of claim 37 further comprising a plurality of die stacks and wherein the component comprises a multi chip module.

41. The semiconductor component of claim 37 wherein the die stack includes a pair of first dice.

42. A semiconductor component comprising:

a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

at least one die stack on the substrate comprising at least two first dice bonded to the substrate with a space therebetween in electrical communication with the interconnect contacts, a first encapsulant encapsulating the at least two first dice and the space, and a second die bonded to the first encapsulant in electrical communication with the interconnect contacts; and

a second encapsulant on the substrate encapsulating the die stack.

43. The semiconductor component of claim 42 wherein the second die has a peripheral outline larger than the at least two first dice.

44. The semiconductor component of claim 42 wherein the at least two first dice and the second die are wire bonded to the interconnect contacts.

45. The semiconductor component of claim 42 wherein the at least two first dice and the second die are TAB bonded to the interconnect contacts.

46. A semiconductor component comprising:

a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

a first die back bonded to the substrate, electrically connected to the interconnect contacts and encapsulated in a first encapsulant;

a second die back bonded to the first encapsulant, electrically connected to the interconnect contacts and encapsulated in a second encapsulant;

a third die back bonded to the second encapsulant, electrically connected to the interconnect contacts; and

a third encapsulant encapsulating the third die and the second encapsulant.

47. The semiconductor component of claim 46 wherein the first encapsulant comprises at least one locking feature configured to increase adhesive bonding of the second die to the first encapsulant.

48. The semiconductor component of claim 46 further a plurality of first interconnects bonded to the first die and to the interconnect contacts, and a plurality of second interconnects bonded to the second die and to the interconnect contacts.

49. The semiconductor component of claim 48 wherein the first interconnects and the second interconnects comprise wire bonded wires.

50. The semiconductor component of claim 48 wherein the first interconnects and the second interconnects comprise TAB bonded tape.

51. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts;

attaching a first die to the substrate;

forming a plurality of first interconnects between the first die and the interconnect contacts;

forming a first encapsulant on the first die and on the first interconnects;

attaching a second die to the first encapsulant;

forming a plurality of second interconnects between the second die and the substrate; and

forming a second encapsulant on the second die, on the second interconnects and on the first encapsulant.

52. The method of claim 51 wherein the first interconnects comprise first wires and the forming the first interconnects step comprises wire bonding.

53. The method of claim 51 wherein the second interconnects comprise second wires and the forming the second interconnects step comprises wire bonding.

54. The method of claim 51 further comprising during the forming the first encapsulant step, forming at least one molded locking feature on the first encapsulant.

55. The method of claim 51 wherein the forming the first encapsulant step comprises molding with a mold cavity configured to prevent an encapsulating material from contaminating selected interconnect contacts.

56. The method of claim 51 further comprising forming a plurality of terminal contacts on the substrate in electrical communication with the interconnect contacts.

57. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

adhesively bonding a first die to the substrate;

electrically connecting the first die to the interconnect contacts;

encapsulating the first die in a first encapsulant having a planar surface;

adhesively bonding a second die to the planar surface;

electrically connecting the second die to the interconnect contacts; and

encapsulating the second die and the first encapsulant in an second encapsulant.

58. The method of claim 57 wherein the encapsulating the first die step comprises transfer molding with a direct gate mold cavity.

59. The method of claim 57 wherein the encapsulating the first die step includes forming at least one locking feature on the planar surface.

60. The method of claim 57 further comprising adhesively bonding a third die to the second encapsulant and encapsulating the third die and the second encapsulant in a third encapsulant.

61. The method of claim 57 wherein the adhesively bonding the first die step comprises forming a first adhesive layer between the first die and the substrate.

62. The method of claim 57 wherein the adhesively bonding the second die step comprises forming a second adhesive layer between the second die and the first encapsulant.

63. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of first interconnect contacts and a plurality of second interconnect contacts;

attaching a first die to the substrate comprising a plurality of first die contacts;

bonding a plurality of first interconnects to the first die contacts and to the first interconnect contacts;

forming a first encapsulant on the first die and the first interconnect contacts while leaving the second interconnect contacts exposed;

bonding a second die to the first encapsulant comprising a plurality of second die contacts;

bonding a plurality of second interconnects to the second die contacts and to the second interconnect contacts; and

forming a second encapsulant on the second die, the second interconnects and the first encapsulant.

64. The method of claim 63 wherein the second interconnect contacts are located proximate to a peripheral edge of the substrate and the second interconnect contacts are located proximate to an inner portion of the substrate.

65. The method of claim 63 wherein the first interconnect contacts and the second interconnect contacts are arranged in spaced rows on opposing edges of the substrate.

66. The method of claim 63 wherein the bonding the first die step comprising forming a first adhesive layer between the first die and the substrate.

67. The method of claim 63 further comprising forming at least one locking feature on the first encapsulant configured to promote adhesion of the second die to the first encapsulant.

68. The method of claim 63 wherein the first interconnects and the second interconnects comprise wire bonded wires.

69. The method of claim 63 wherein the first interconnects and the second interconnects comprise bonded TAB tape.

70. The method of claim 63 further comprising forming a plurality of terminal contacts on the substrate in electrical communication with the first interconnect contacts and the second interconnect contacts.

71. The method of claim 63 further comprising bonding a third die to the second encapsulant and forming a third encapsulant on the third die and the second encapsulant.

72. The method of claim 63 wherein the forming the first encapsulant step comprises transfer molding with a direct gate mold cavity.

73. The method of claim 63 wherein the forming the first encapsulant step comprises molding at least one locking feature on the first encapsulant configured to facilitate bonding of the second die to the first encapsulant.

74. The method of claim 63 wherein the forming the first encapsulant step comprises injection molding.

75. The method of claim 63 wherein the forming the first encapsulant step comprises deposition of a viscous plastic through a nozzle.

76. The method of claim 63 wherein the forming the first encapsulant step comprises stereo lithography.

77. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

forming a plurality of die stacks on the substrate, each die stack comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die, and a second die bonded to the first encapsulant in electrical communication with the interconnect contacts; and

forming a second encapsulant on the substrate encapsulating the die stacks.

78. The method of claim 77 wherein the forming the die stacks step comprises wire bonding the first die and the second die to the interconnect contacts.

79. The method of claim 77 wherein the forming the die stacks step comprises TAB bonding the first die and the second die to the interconnect contacts.

80. The method of claim 77 wherein the forming the die stacks step comprises transfer molding the first encapsulant with a direct gate mold cavity configured to not contaminate selected interconnect contacts.

81. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

back bonding a first die to the substrate;

electrically bonding the first die to the interconnect contacts;

encapsulating the first die in a first encapsulant;

back bonding a second die to the first encapsulant;

electrically bonding the second die to the interconnect contacts;

encapsulating the second die in a second encapsulant;

back bonding a third die to the second encapsulant;

electrically bonding the third die to the interconnect contacts; and

encapsulating the third die and the second encapsulant in a third encapsulant.

82. The method of claim 81 wherein the first encapsulant comprises at least one locking feature configured to facilitate bonding of the second die to the first encapsulant.

83. The method of claim 81 wherein the electrically bonding the first die step, the electrically bonding the second die step, and the electrically bonding the third die step comprise wire bonding.

84. The method of claim 81 wherein the electrically bonding the first die step, the electrically bonding the second die step, and the electrically bonding the third die step comprise TAB bonding.

85. A system comprising:

a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts; and

a die stack on the substrate comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die, a second die bonded to the first encapsulant in electrical communication with the interconnect contacts, and a second encapsulant encapsulating the second die and the first encapsulant.

86. The system of claim 85 further comprising a plurality of die stacks on the substrate.

87. The system of claim 85 wherein the substrate is contained in a computer.

88. The system of claim 85 wherein the substrate is contained in a camcorder.

89. The system of claim 85 wherein the substrate is contained in a camera.

90. The system of claim 85 wherein the substrate is contained in a cell phone.

91. The system of claim 85 wherein the substrate is contained in a medical device.

92. The system of claim 85 wherein the first encapsulant comprises at least one locking feature configured to increase adhesive bonding of the second die to the first encapsulant.

93. The system of claim 85 wherein the die stack comprises a third die bonded to the second encapsulant, and a third encapsulant encapsulating the third die and the second encapsulant.

94. The system of claim 85 further comprising a plurality of die stacks on the substrate.

95. The system of claim 85 wherein the substrate and the die stack comprise a multi chip module.